What is claimed is:

1. An MTCMOS flip-flop circuit, comprising:

a master latch unit to latch input data and output the data under the control of an internal clock;

a slave latch unit for latching input data and outputting the data under the control of an internal clock signal;

wherein an output of the flip-flop circuit retains a state just before admission to a sleep mode when the state of the system is converted from sleep mode to an active mode by means of making a data state of an input terminal of the master latch circuit into the same state as an inversed data state of an input terminal of the slave latch circuit in sleep mode and storing the data state of the input terminal of the master latch circuit.

2. The MTCMOS flip-flop circuit according to claim 1, wherein the MTCMOS flip-flop circuit comprises a switching transistor connected between a virtual ground and a ground, which is turned on by a sleep mode control signal in sleep mode and turned off by the sleep mode control signal in active mode.

3. The MTCMOS flip-flop circuit according to claim 1, wherein the MTCMOS flip-flop circuit comprises a data retention feedback circuit for inverting data from the input terminal of the slave latch circuit under the control of an inverted sleep mode control signal, and outputting the data to the input terminal of the master latch circuit, thereby retaining a state just before the admission to sleep mode of an output of the flip-flop circuit when the state of the system is converted from sleep mode to active mode.

4. The MTCMOS flip-flop circuit according to claim 3, wherein the data retention feedback circuit comprises:

a first inverter for inverting the inverted sleep mode control signal;

a first PMOS transistor having a source terminal connected to a power supply voltage, and a gate terminal to which an output signal of the first inverter is applied;

a second PMOS transistor having a source terminal connected to a drain terminal of the first PMOS transistor, a gate terminal connected to the input terminal of the slave latch

circuit for receiving a feedback input signal, and a drain terminal connected to the input terminal of the master latch circuit for outputting a feedback output signal;

a first NMOS transistor having a drain terminal connected to a drain terminal of the second PMOS transistor, and a gate terminal connected to a gate terminal of the second PMOS transistor; and

a second NMOS transistor having a drain terminal connected to the source terminal of the first NMOS transistor, and a source terminal connected to a ground of the gate terminal to which the inverted sleep mode control signal is applied.

5. The MTCMOS flip-flop circuit according to claim 1, wherein the master latch unit is consisted of a high-Vth transistor, and the slave latch unit is consisted of a low-Vth transistor.

6. The MTCMOS flip-flop circuit according to claim 1, wherein the internal clock signal does not oscillate depending upon the external clock signal in sleep mode, and oscillates in response to the external clock signal in active mode.

7. The MTCMOS flip-flop circuit according to claim 1, wherein the MTCMOS flip-flop circuit is provided with a sleep mode control circuit for retaining the clock signal in low state regardless of an external clock signal in sleep mode, and outputting an inverted signal of the external clock signal as the internal clock signal in active mode.

8. The MTCMOS flip-flop circuit according to claim 7, wherein the sleep mode control circuit comprises:

a first PMOS transistor having a source terminal connected to a power supply voltage, and a gate terminal for receiving an inverted sleep mode control signal;

a second PMOS transistor having a source terminal connected to the drain terminal of the first PMOS transistor, a gate terminal for receiving an external clock signal, and a drain terminal connected to a first node;

a first NMOS transistor having a drain terminal connected to the first node, a gate terminal for receiving the external clock signal, and a source terminal connected to a ground; and

a second NMOS transistor having a drain terminal connected to the first node, a gate terminal for receiving the inverted sleep mode control signal, and a source terminal connected to a ground, wherein the first node generates the internal clock signal.

9. The MTCMOS flip-flop circuit according to claim 8, wherein the first PMOS transistor is a high-Vth transistor, and the second PMOS transistor, the first NMOS transistor and the second NMOS transistor are low-Vth transistor.

10. An MTCMOS flip-flop circuit comprising:

a sleep mode control circuit for receiving an external clock signal and an inverted sleep mode control signal and generating an internal clock signal;

a first inverter for inverting flip-flop input data;

a master latch gate for receiving an output signal of the first inverter and transmitting to a first node under control of the internal clock signal and the inverted internal clock signal;

a master latch circuit for receiving and latching an output signal of the master lach gate and outputting the signal to a second node;

a slave latch gate for receiving a signal of the second node and transmitting the signal to a third node under the control of the internal clock signal and the inverted clock signal;

a slave latch circuit for receiving and latching an output signal of the slave latch gate, and outputting the signal to a fourth node; and

a data retention feedback circuit for receiving a feedback input signal from the third node under control of the inverted sleep mode control signal and transmitting the feedback output signal to the first node.

11. The MTCMOS flip-flop circuit according to claim 10, wherein the MTCMOS flip-flop circuit is further provided with a switching transistor connected between a virtual ground and a ground, which is turned on by a sleep mode control signal in sleep mode and turned off by the sleep mode control signal in active mode.

12. The MTCMOS flip-flop circuit according to claim 10, wherein the MTCMOS flip-flop circuit is further provided with a buffer circuit for inverting an output signal of the slave latch circuit, and buffering the signal, and generating a flip-flop output signal.

13. The MTCMOS flip-flop circuit according to claim 10, wherein the data retention feedback circuit comprises:

a first inverter for receiving the inverted sleep mode control signal and inverting the signal;

a first PMOS transistor having a source terminal connected to a power supply voltage, and a gate terminal which an output signal of the first inverter is applied;

a second PMOS transistor having a source terminal connected to a drain terminal of the first PMOS transistor, a gate terminal, connected to the input terminal of the slave latch circuit, for receiving a feedback input signal, and a drain terminal, connected to the input terminal of the master latch circuit, for outputting a feedback output signal;

a first NMOS transistor having a drain terminal connected to the drain terminal of the second PMOS transistor, and a gate terminal connected to the gate terminal of the second PMOS transistor; and

a second NMOS transistor having a drain terminal connected to the source terminal of the first NMOS transistor, and a source terminal connected to a ground of the gate terminal which the inverted sleep mode control signal is applied.

14. The MTCMOS flip-flop circuit according to claim 10 , wherein the sleep mode control circuit comprises:

a first PMOS transistor having a source terminal connected to a power supply voltage, and a gate terminal for receiving an inverted sleep mode control signal;

a second PMOS transistor having a source terminal connected to the drain terminal of the first PMOS transistor, a gate terminal for receiving the external clock signal, and a drain terminal connected to a fifth node;

a first NMOS transistor having a drain terminal connected to the fifth node, a gate terminal for receiving the external clock signal, and a source terminal connected to a ground; and

a second NMOS transistor having a drain terminal connected to the fifth node, a gate terminal for receiving the inverted sleep mode control signal, and a source terminal connected to a ground, wherein the fifth node generates the internal clock signal.

15. The MTCMOS flip-flop circuit according to claim 11, wherein the master latch gate is a first transmitting gate consisted of a high-Vth transistor, and the master latch gate becomes "on" when the internal clock signal is in high state.

16. The MTCMOS flip-flop circuit according to claim 11, wherein the master latch circuit comprises:

a second inverter for inverting a signal of the first node, and outputting the signal to the second node;

a third inverter for inverting a signal of the second node; and

a second transmitting gate for receiving an output signal of the third inverter and transmitting the signal to the first node under the control of the internal clock signal and the inverted internal clock signal.

17. The MTCMOS flip-flop circuit according to claim 16, wherein the second transmitting gate becomes "on" when the internal clock signal is in low state.

18. The MTCMOS flip-flop circuit according to claim 16, wherein the second transmitting gate, the second inverter and the third inverter are consisted of a high-Vth transistor.

19. The MTCMOS flip-flop circuit according to claim 10, wherein the slave latch gate is a third transmitting gate consisted of a low-Vth transistor, and the slave latch gate becomes "on" when the internal clock signal is in high state.

20. The MTCMOS flip-flop circuit according to claim 10, wherein the slave latch circuit comprises:

a fourth inverter for inverting a signal of the third node, and outputting the signal to the fourth node;

a fifth inverter for inverting a signal of the fourth node; and

a fourth transmitting gate for receiving an output signal of the fifth inverter and transmitting the signal to the third node under the control of the internal clock signal and the inverted internal clock signal.

21. The MTCMOS flip-flop circuit according to claim 20, wherein the fourth transmitting gate becomes "on" when the internal clock signal is in high state.

22. The MTCMOS flip-flop circuit according to claim 20, wherein the second transmitting gate is consisted of a high-Vth transistor, and the fourth inverter and the fifth inverter are consisted of a low-Vth transistor.